

Application No.: 09/899,994
Amendment under 37 CFR 1.111
Reply to Office Action dated June 14, 2004
September 14, 2004

REMARKS

By this amendment, the specification has been editorially amended and claims 1, 4-7 and 11-18 have been amended. Currently, claims 1-19 are pending in the application.

The Examiner stated that the title of the invention was not descriptive. By this amendment, the title "SIGNAL PROCESSING UNIT AND SIGNAL PROCESSING METHOD" has been amended to "SIGNAL PROCESSING DEVICE AND SIGNAL PROCESSING METHOD INCLUDING RE-SAMPLING AND A DELAY UNIT". It is respectfully submitted that this objection should be withdrawn in view of this amendment.

The Examiner stated that claim 4 was objected to because the term "of" should be deleted. By this amendment, the term "of" has been deleted in claim 4. It is respectfully submitted that this objection should be withdrawn in view of this amendment.

Claims 1-3, 5-7, 12-14 and 16 were rejected under 35 USC 103(a) as being obvious over Curley et al. in view of Dieterich. Further, claims 4 and 15 were rejected under 35 USC 103(a) as being obvious over Curley et al. in view of Dieterich and further in view of Dattorro et al. Also, claims 8-11 and 17-19 were rejected under

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35 USC 103(a) as being obvious over Curley et al. in view of Dieterich and further in view of Duan et al.

These rejections are respectfully traversed in view of the following remarks.

The present invention relates to a signal processing device and method which perform signal processing for reproducing multi-channel audio data that has been recorded on an optical disk or the like, without generating a delay time difference between a plurality of streams of audio data digitized at different sampling frequencies.

Specifically, embodiment 1 discloses that the decoding circuit 16 is a circuit which inputs, via a terminal 7, a data stream D3 in which the first and second audio data have been encoded and combined by an encoding circuit like the encoding circuit 5 of Fig. 1. By referring to the header data, the circuit separates the data stream D3 into a first audio data D1 and a second audio data D2 and decodes them. This process returns them to respective audio data at sampling frequencies fs1 and fs2. The buffer 9 is a device for temporarily storing the first audio data D1 and the buffer 10 is a device for temporarily storing the second audio data D2.

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The output data from the buffer 9 is input to the up-sampling circuit 17. The up-sampling circuit 17 performs up-sampling upon this inputted data at approximately twice the sampling frequency, in consideration of the number of data elements (in this case 80) in one block of the second audio data D2. If for example the FIR filter 17b is used in the up-sampling circuit 17, then its delay amount will be equal to $(N+1)/2$ in terms of the tap number N of the FIR filter 17b. Accordingly, if the number of data elements in the second audio data D2 is supposed to be 80, then the characteristics of the FIR filter 17b are set so that its tap number N should be equal to 159, in order for this delay amount to become adequate for 80 samples..

On the other hand, the output data elements from the buffer 10 are input to the delay buffer 18. This delay buffer 18 generates the delay period of one block by storing the number of data elements in one block (= 80 data elements). The delay buffer 18 has a structure as shown in Figs. 7A and 7B. Fig. 7A shows the input-output state at a certain time point, while Fig. 7B shows the input-output state at the next clock signal. When one data $N1$ is input, the delay buffer 18 outputs the data element 01 among the previously stored data elements 01 to 80.

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Actually, the input data N1 is input at a clock rate which is synchronized with the sampling frequency. The delay amount of the signal is easily controlled in this manner by making the tap number of the FIR filter in the up-sampling circuit 17 equal to the number of data elements in one block of audio data which is input.

The output of the up-sampling circuit 17 is converted into an analog signal by the D/A converter 12, and is output via the output terminal 14 to the outside. Moreover, the output of the delay buffer 18 is converted into an analog signal by the D/A converter 13, and is output via the output terminal 15 to the outside. By this type of processing, the two streams of audio signals are output so that their phases coincide.

When this type of signal processing method is applied to multi-channel DVD audio, no phase difference or time difference is generated in the output sound, even when, for example, the sampling frequency fs_2 for the forward left channel and right channel signals is 96 kHz or 88.2 kHz while the sampling frequency fs_1 for the surround-sound signals including the backward signals is 48 kHz or 44.1 kHz. Due to this structure

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and arrangement it is possible to obtain the same sound field effect as the originally recorded audio.

Independent claim 1 has been amended to recite "a decoder for receiving and separating the data stream into the first audio data and the second audio data and for outputting the first audio data and the second audio data; a filter for performing re-sampling upon the first audio data at the same sampling frequency fs_2 as that of the second audio data, and suppressing aliasing distortion due to the re-sampling, and for outputting the first audio data from the filter; and a delay unit for delaying the second audio data by a delay period equal to a processing period due to the filter, and for outputting the second audio data concurrently with the first audio data". Similarly, independent claim 12 has been amended to recite "decoding the data stream and separating the data stream into the first audio data and the second audio data and outputting the first audio data and the second audio data; filtering the first audio data by re-sampling at the same sampling frequency fs_2 as that of the second audio data, and suppressing aliasing distortion in the first audio data obtained following the step of re-sampling, and outputting the first audio data; and delaying the second audio data by a delay

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period equal to a processing period due to the step of filtering to output the second audio data concurrently with the first audio data".

Curley et al. relate to digital data decoding systems and more particularly, to a processing facility capable of receiving multiple concurrent streams of digital audio data and simultaneously outputting therefrom both a mixed digital audio signal and an unmixed digital audio signal.

Curley et al. discloses that the encoded primary stream of data is decoded by a stream decode capability 24 of the system and the resultant decoded data is output as an unmixed digital audio signal.

Curley et al. also discloses that a secondary stream of audio digital data is received through a second interface 22 and in this embodiment, undergoes resampling 26. The resampling logic 26 also receives as input a frequency control signal derived from the sample frequency of the primary stream of digital data. This redigitization function causes a second stream of audio digital data to be resampled at a sample rate of a first stream of audio digital data.

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Curley et al. also disclose that if the secondary stream of audio digital data has the same sampling rate as the primary stream of digital audio data, then no resampling is necessary.

Curley et al. do not disclose a decoder for receiving and separating the data stream into the first audio data and the second audio data and for outputting the first audio data and the second audio data; a filter for performing re-sampling upon the first audio data at the same sampling frequency fs_2 as that of the second audio data, and suppressing aliasing distortion due to the re-sampling, and for outputting the first audio data from the filter; and a delay unit for delaying the second audio data by a delay period equal to a processing period due to the filter, and for outputting the second audio data concurrently with the first audio data as claimed in claim 1.

Curley et al. also do not disclose decoding the data stream and separating the data stream into the first audio data and the second audio data and outputting the first audio data and the second audio data; filtering the first audio data by re-sampling at the same sampling frequency fs_2 as that of the second audio data, and suppressing aliasing distortion in the first audio data obtained following the step of re-sampling, and outputting the

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first audio data; and delaying the second audio data by a delay period equal to a processing period due to the step of filtering to output the second audio data concurrently with the first audio data as claimed in claim 12.

Also, applicants respectfully submit Curley et al. do not disclose the decoder and delay unit as claimed in claims 1 and 12. The device disclosed by Curley et al. simply outputs two types of audio data simultaneously, but does not touch upon the timing correction of those two types of data. The decoder of amended claim 1 divides an inputted data stream into first and second audio data by a processing unit corresponding to the processing period in the filter. The delay unit of the present invention delays the second audio data so as to output the first and second audio data concurrently.

For these reasons, it is believed that Curley et al. do not show or suggest the present claimed features of the present invention. Applicants also submit that Dieterich does not make up for the deficiencies in Curley et al.

Dieterich relates to a disc record player for recovering an audio signal recorded in digital and analog format on high density disc records.

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Dieterich discloses a digital/analog converter that reduces the decoded signal to a first analog manifestation of the recorded audio signal. Delay circuitry is incorporated within the foregoing circuitry to temporally align the resultant analog audio signal with the recorded time displaced analog audio signal.

Dieterich also discloses that a signal generated in the audio source 20, e.g., the left plus right (L+R) stereo channel, is also applied to a delay element 29 which time displaces this signal with respect to its digital counterpart. Element 29 may be an analog charge transfer device as, for example, a serial charge coupled device (CCD) delay line.

Dieterich also discloses that the delayed signal is applied to circuitry 27 for modulating a second carrier frequency generated by stable oscillator 28. The second carrier frequency is considerably lower in Hertz than the first carrier frequency, i.e., the ratio of frequencies is approximately 1:10 with the higher frequency carrier centered about 5 MHz, for example. The two modulated carriers are linearly combined in circuitry 25 and subsequently conditioned in amplifier 26 for recording on a master disc 100.

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Dieterich does not disclose a decoder for receiving and separating the data stream into the first audio data and the second audio data and for outputting the first audio data and the second audio data; a filter for performing re-sampling upon the first audio data at the same sampling frequency fs_2 as that of the second audio data, and suppressing aliasing distortion due to the re-sampling, and for outputting the first audio data from the filter; and a delay unit for delaying the second audio data by a delay period equal to a processing period due to the filter, and for outputting the second audio data concurrently with the first audio data as claimed in claim 1.

Dieterich also does not decoding the data stream and separating the data stream into the first audio data and the second audio data and outputting the first audio data and the second audio data; filtering the first audio data by re-sampling at the same sampling frequency fs_2 as that of the second audio data, and suppressing aliasing distortion in the first audio data obtained following the step of re-sampling, and outputting the first audio data; and delaying the second audio data by a delay period equal to a processing period due to the step of filtering

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to output the second audio data concurrently with the first audio data as claimed in claim 12.

Also, applicants respectfully submit Dieterich does not disclose re-sampling the audio data. Applicants also submit that it is not obvious to combine Curley et al. with Dieterich and to obtain the device as the present invention.

For these reasons, it is believed that Dieterich does not show or suggest the present claimed features of the present invention.

Applicants also respectfully submit that Dattorro et al. do not make up for the deficiencies in Curley et al. and Dieterich.

Dattorro et al. relate to digital filters and in particular to a digital decimation filter suitable for use in a sigma-delta analog-to-digital converter.

Dattorro et al. disclose a single stage FIR decimation filter, having 2048 coefficients, low-pass filters and decimates the signal provided by the modulator to produce a digital output signal having a sampling rate of 48 KHz and having equivalent resolution to a sampled data signal provided by a 16 bit flash analog-to-digital converters (ADC).

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Dattorro et al. also disclose the decimation filter employs 32 digital FIR filters configured in parallel as single multirate filter. The output signals provided by the 32 filters are staggered in time such that each filter provides sample values at a rate of 48 KHz/32 or 1.5 KHz. These output sample values are combined by commutation to produce an output signal having a sampling frequency of 48KHz.

Dattorro et al. do not disclose a decoder for receiving and separating the data stream into the first audio data and the second audio data and for outputting the first audio data and the second audio data; a filter for performing re-sampling upon the first audio data at the same sampling frequency fs_2 as that of the second audio data, and suppressing aliasing distortion due to the re-sampling, and for outputting the first audio data from the filter; and a delay unit for delaying the second audio data by a delay period equal to a processing period due to the filter, and for outputting the second audio data concurrently with the first audio data as claimed in claim 1.

Dattorro et al. also do not decoding the data stream and separating the data stream into the first audio data and the second audio data and outputting the first audio data and the

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second audio data; filtering the first audio data by re-sampling at the same sampling frequency fs_2 as that of the second audio data, and suppressing aliasing distortion in the first audio data obtained following the step of re-sampling, and outputting the first audio data; and delaying the second audio data by a delay period equal to a processing period due to the step of filtering to output the second audio data concurrently with the first audio data as claimed in claim 12.

For these reasons, it is believed that Dattorro et al. do not show or suggest the present claimed features of the present invention.

Applicants also submit that Duan et al. do not make up for the deficiencies in Curley et al., Dieterich and Dattorro et al.

Duan et al. relate to the field of digital signal processing and in particular to the field of audio signal synchronization and mixing.

Duan et al. disclose Fig. 2A which illustrates an example of a system for synchronizing and mixing multiple streams at different sampling rates. The ovals 210, 220, 230, 240, 260 and 270 represent buffers for receiving samples for input streams S1-S7, respectively. The ovals 215, 225, 235, 245, 255 and 265 represent

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intermediate buffers and the oval 275 represents an output buffer. The upper line in each oval, A-G, 6A, 3B, 3C/2, 640D/147, 160F/147 and Q, each represent the size of the buffer. If the expression given is not an integer, the size of the buffer is the next larger integer. That is, if the expressed size is $3\frac{1}{4}$, the size of the buffer is 4. The lower line in each oval, 8k, 16k, 32k, 11.035k, 22.05k, 44.1k and 48k represents the sample rate corresponding to the samples in each buffer.

Duan et al. disclose that the rectangular blocks 310-360 represent upsamplers that scale the sampling rate and the corresponding number of samples by the ratio shown in each block. In a preferred embodiment, the upsamplers can be fractional filters.

Duan et al. do not disclose a decoder for receiving and separating the data stream into the first audio data and the second audio data and for outputting the first audio data and the second audio data; a filter for performing re-sampling upon the first audio data at the same sampling frequency fs_2 as that of the second audio data, and suppressing aliasing distortion due to the re-sampling, and for outputting the first audio data from the filter; and a delay unit for delaying the second audio data by a

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delay period equal to a processing period due to the filter, and for outputting the second audio data concurrently with the first audio data as claimed in claim 1.

Duan et al. also do not disclose decoding the data stream and separating the data stream into the first audio data and the second audio data and outputting the first audio data and the second audio data; filtering the first audio data by re-sampling at the same sampling frequency fs_2 as that of the second audio data, and suppressing aliasing distortion in the first audio data obtained following the step of re-sampling, and outputting the first audio data; and delaying the second audio data by a delay period equal to a processing period due to the step of filtering to output the second audio data concurrently with the first audio data as claimed in claim 12.

It is respectfully submitted that Curley et al., Dieterich, Dattorro et al. and Duan et al., individually or in combination, do not teach, disclose or suggest the presently claimed invention and it would not have been obvious to one of ordinary skill in the art to combine these references to render the present claims obvious. Additionally, there is no teaching or suggestion in

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Curley et al. and Dieterich for combining these references as suggested by the Examiner.

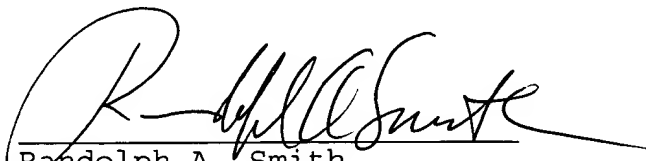
In view of foregoing claim amendments and remarks, it is respectfully submitted that the application is now in condition for allowance and an action to this effect is respectfully requested.

Applicants also respectfully submit that the amendments to claims 1, 4-7 and 11-18 were to clarify the claim language and were not done for reasons related to patentability.

If there are any questions or concerns regarding the amendments or these remarks, the Examiner is requested to telephone the undersigned at the telephone number listed below.

Respectfully submitted,

Date: September 14, 2004


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